

**N-CHANNEL ENHANCEMENT MODE FIELD MOSFET**
**Product Summary**

$V_{(BR)SSS}$	$R_{SS(ON)}$	Package	$I_S$ $T_A = +25^\circ C$
24V	26m $\Omega$ @ $V_{GS} = 4.5V$	X1-WLB1818-4	6.0A

**Description**

This new generation MOSFET is designed to minimize the on-state resistance ( $R_{SS(ON)}$ ) with thin WLCSP packaging process and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

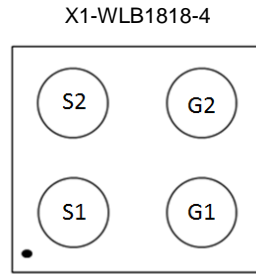
- Battery Management
- Load Switch
- Battery Protection

**Features**

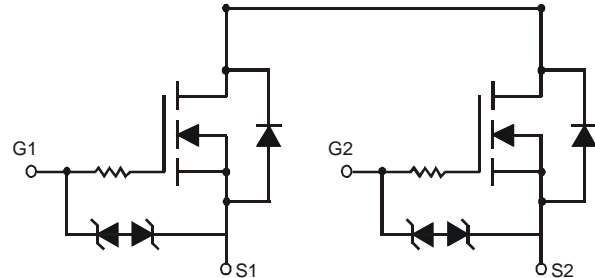
- Built-in G-S Protection Diode Against ESD 2kV HBM
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: X1-WLB1818-4
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram



Top View



Equivalent Circuit

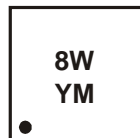
**Ordering Information** (Note 4)

Part Number	Case	Packaging
DMN2023UCB4-7	X1-WLB1818-4	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

**Marking Information**

X1-WLB1818-4



8W = Product Type Marking Code  
 YM = Date Code Marking  
 Y or  $\underline{Y}$  = Year (ex: E = 2017)  
 M or  $\underline{M}$  = Month (ex: 9 = September)

## Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Source-Source Voltage			V <sub>SSS</sub>	24	V
Gate-Source Voltage (Note 5)			V <sub>GSS</sub>	±12	V
Continuous Source Current @ T <sub>A</sub> = +25°C (Note 6)	Steady State	T <sub>A</sub> = +25°C	I <sub>S</sub>	6.0	A
		T <sub>A</sub> = +70°C		4.8	
Pulsed Source Current @ T <sub>A</sub> = +25°C (Notes 6 & 7)			I <sub>SM</sub>	20	A

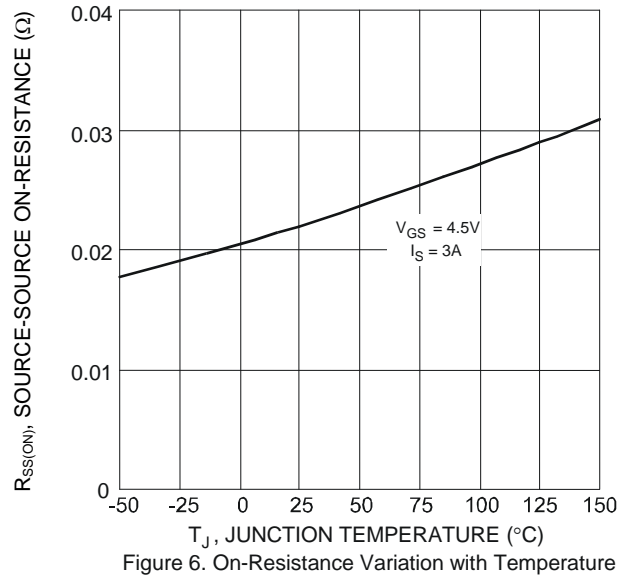
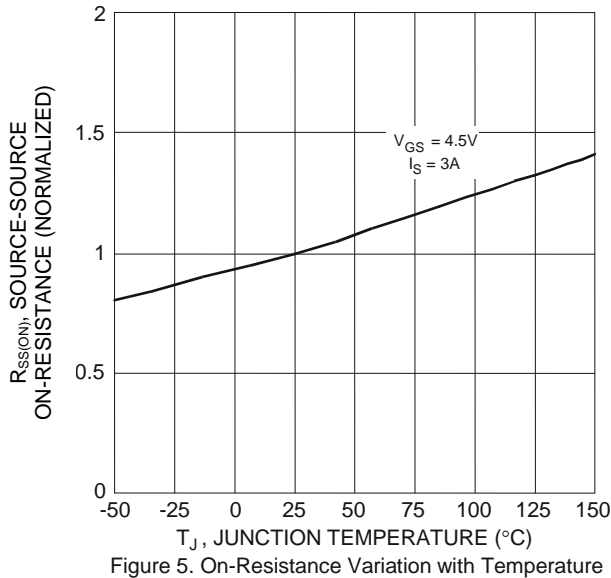
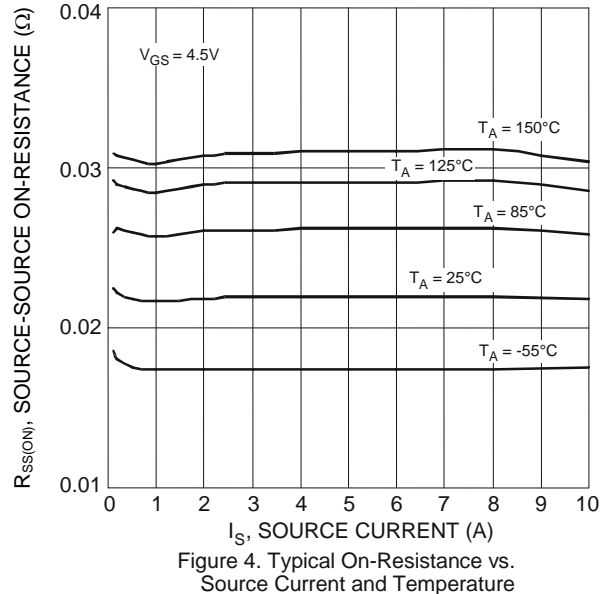
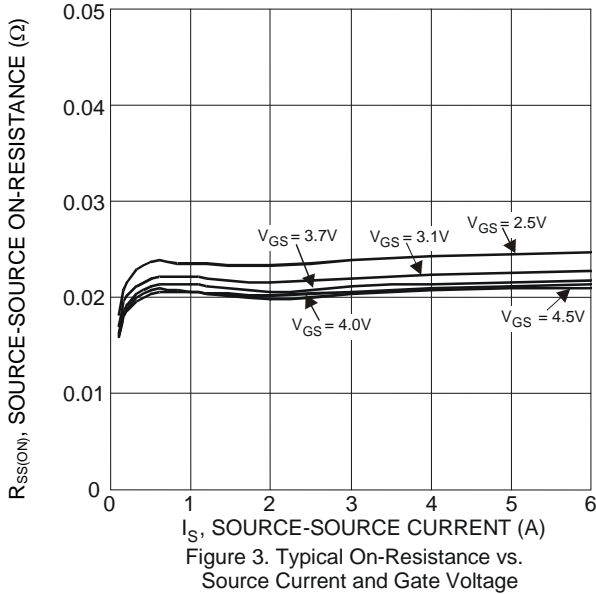
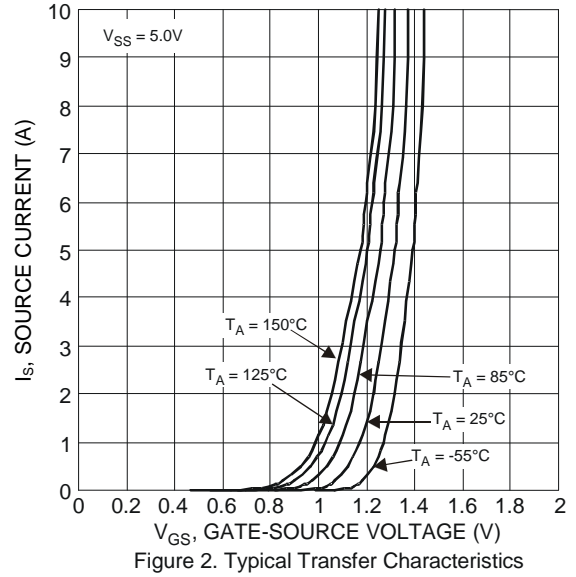
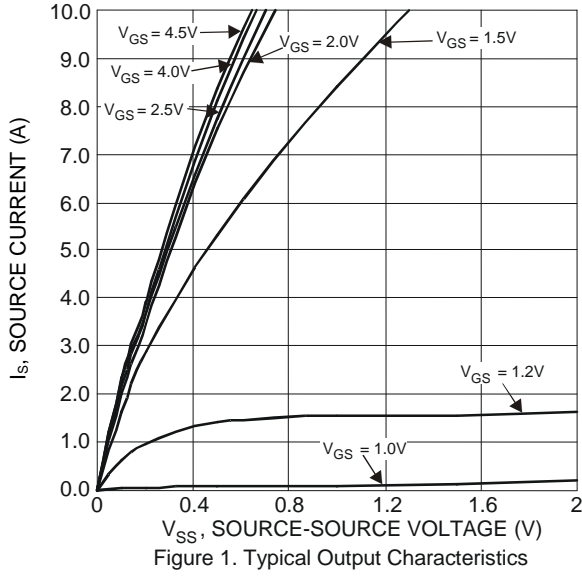
**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation @ T <sub>A</sub> = +25°C (Note 6)	P <sub>D</sub>	1.45	W
Thermal Resistance, Junction to Ambient @ T <sub>A</sub> = +25°C (Note 6)	R <sub>θJA</sub>	88.21	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Source to Source Breakdown Voltage T <sub>J</sub> = +25°C	V <sub>(BR)SSS</sub>	24	—	—	V	I <sub>S</sub> = 1mA, V <sub>GS</sub> = 0V, Test Circuit 1
Zero Gate Voltage Source Current T <sub>J</sub> = +25°C	I <sub>SSS</sub>	—	—	1.0	µA	V <sub>SS</sub> = 20V, V <sub>GS</sub> = 0V, Test Circuit 1
Gate-Body Leakage	I <sub>GSS</sub>	—	—	±10	µA	V <sub>GS</sub> = ±8V, V <sub>SS</sub> = 0V, Test Circuit 2
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.5	—	1.3	V	V <sub>SS</sub> = 10V, I <sub>S</sub> = 1.0mA, Test Circuit 3
Static Source-Source On-Resistance	R <sub>SS(ON)</sub>	17	21.5	25.5	mΩ	V <sub>GS</sub> = 6.5V, I <sub>S</sub> = 3.0A, Test Circuit 5
		17.5	22	26		V <sub>GS</sub> = 4.5V, I <sub>S</sub> = 3.0A, Test Circuit 5
		18.5	23	27		V <sub>GS</sub> = 4.0V, I <sub>S</sub> = 3.0A, Test Circuit 5
		19	23.5	29		V <sub>GS</sub> = 3.7V, I <sub>S</sub> = 3.0A, Test Circuit 5
		19.5	24	33		V <sub>GS</sub> = 3.1V, I <sub>S</sub> = 3.0A, Test Circuit 5
		21.5	27	40		V <sub>GS</sub> = 2.5V, I <sub>S</sub> = 3.0A, Test Circuit 5
Forward Transfer Admittance	Y <sub>fs</sub>	—	12	—	S	V <sub>SS</sub> = 10V, I <sub>S</sub> = 3.0A, Test Circuit 4
Body Diode Forward Voltage	V <sub>F(S-S)</sub>	—	0.7	1	V	I <sub>F</sub> = 3.0A, V <sub>GS</sub> = 0V, Test Circuit 6
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	—	2564	3333	pF	V <sub>SS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1.0MHz Test Circuit 7
Output Capacitance	C <sub>oss</sub>	—	197	275		
Reverse Transfer Capacitance	C <sub>riss</sub>	—	183	260		
Total Gate Charge	Q <sub>g</sub>	—	29	37	nC	V <sub>GS</sub> = 4.5V, V <sub>SS</sub> = 10V, I <sub>S</sub> = 6A Test Circuit 9
Turn-On Delay Time	t <sub>D(ON)</sub>	—	10	15	ns	V <sub>SS</sub> = 10V, R <sub>L</sub> = 3.33Ω, I <sub>S</sub> = 3.0A Test Circuit 8
Turn-On Rise Time	t <sub>R</sub>	—	20	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	75	110	ns	
Turn-Off Fall Time	t <sub>F</sub>	—	29	—	ns	

- Notes:
- AEC-Q101 V<sub>GS</sub> maximum is ±9.6V.
  - Device mounted on FR-4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz.(0.071-mm thick) Cu.
  - Repetitive rating, pulse width limited by junction temperature.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.



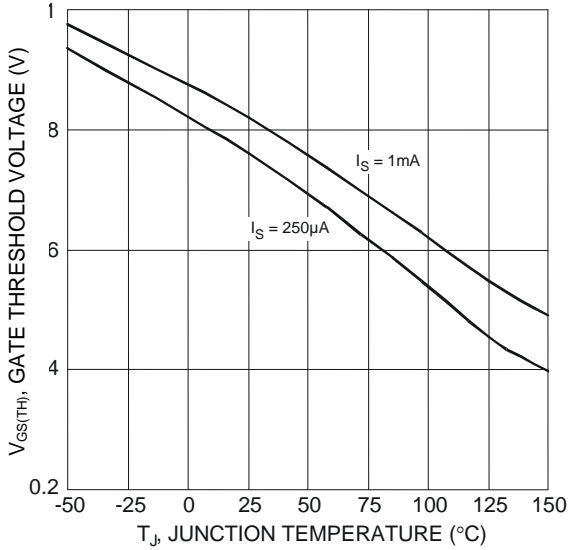


Figure 7. Gate Threshold Variation vs. Junction Temperature

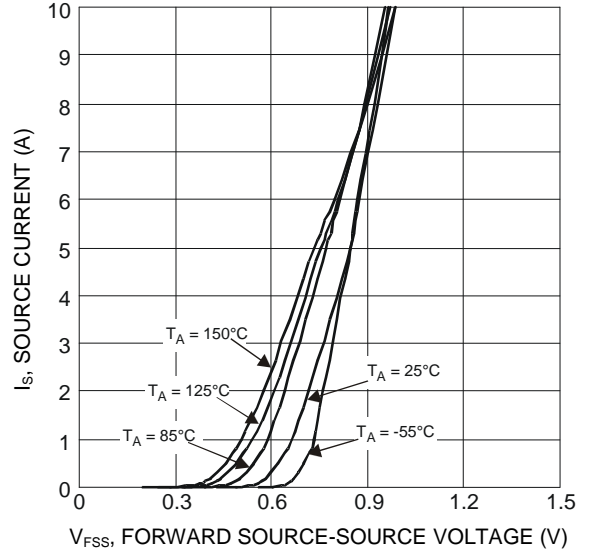


Figure 8. Diode Forward Voltage vs. Current

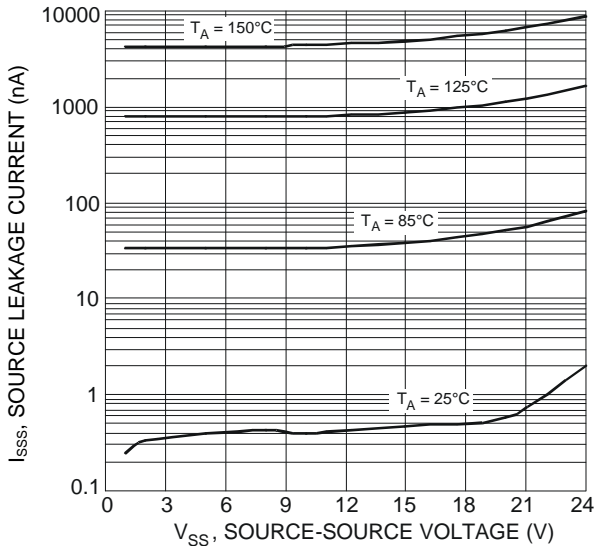


Figure 9. Typical Source-Source Leakage Current vs. Voltage

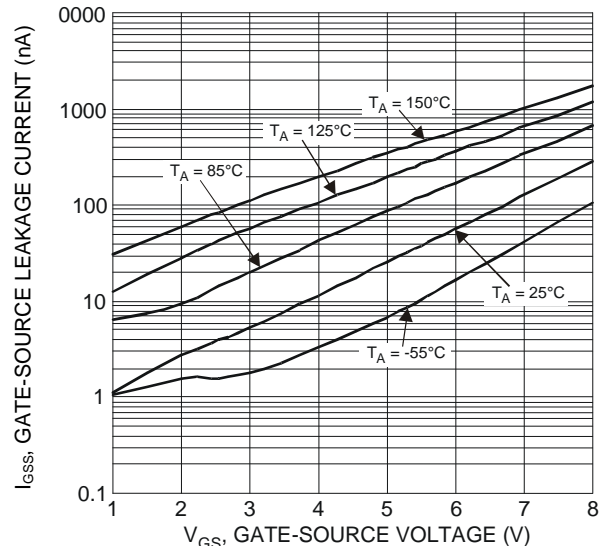


Figure 10. Typical Gate-Source Leakage Current vs. Gate-Source Voltage

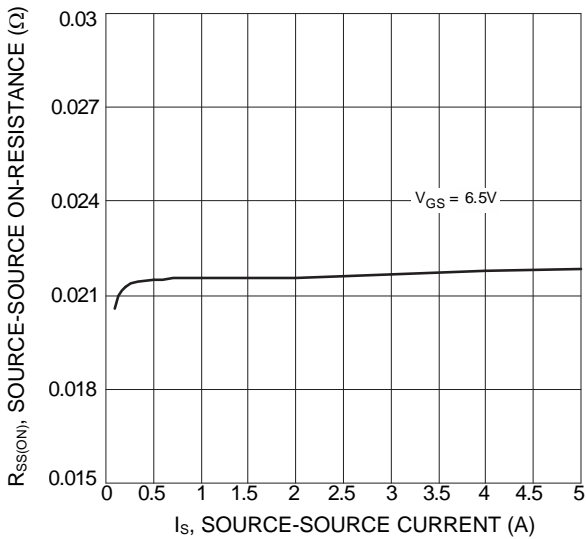


Figure 11. Typical On-Resistance vs. Source Current and Gate Voltage

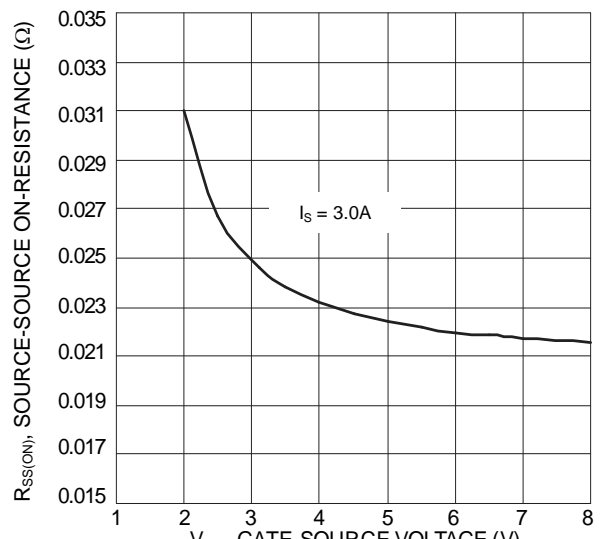
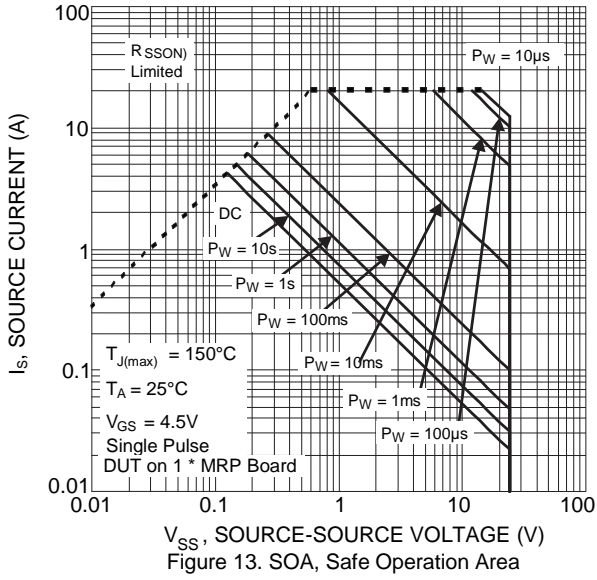
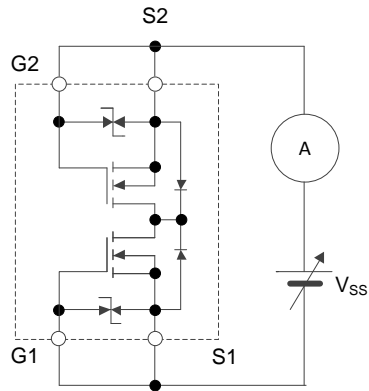


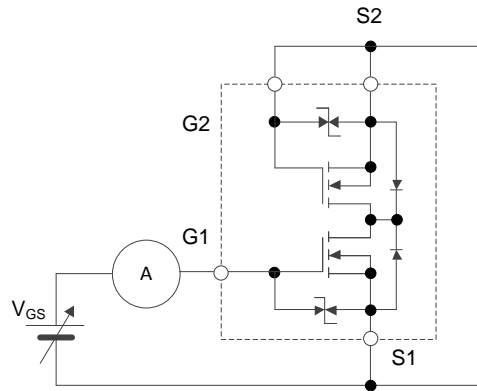
Figure 12. Typical Transfer Characteristic



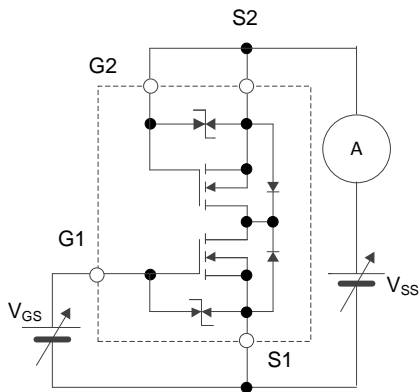
**Test Circuits**



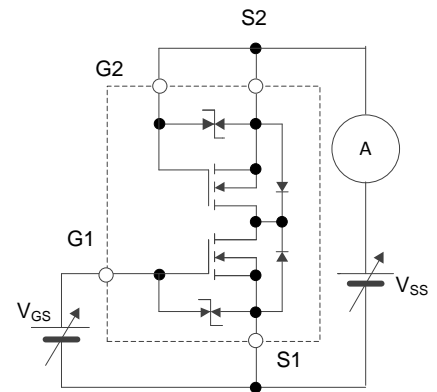
Test Circuit 1  $I_{SSS}$



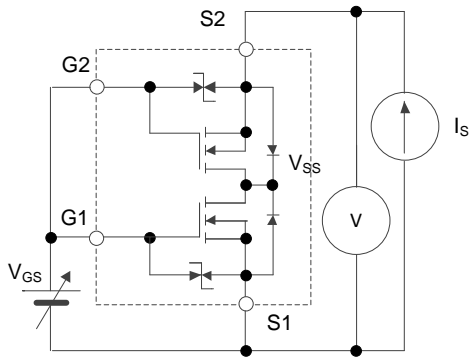
Test Circuit 2  $I_{GSS}$   
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



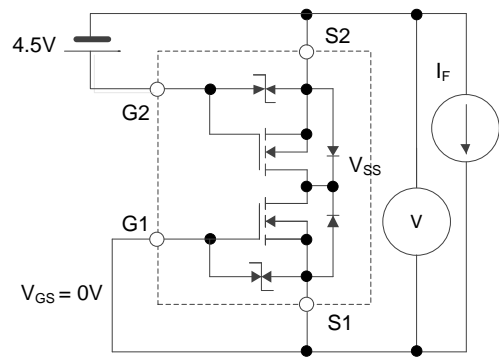
Test Circuit 3  $V_{GS(OFF)}$   
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



Test Circuit 4  $|Y_{fs}|$   
 $\Delta I_S / \Delta V_{GS}$

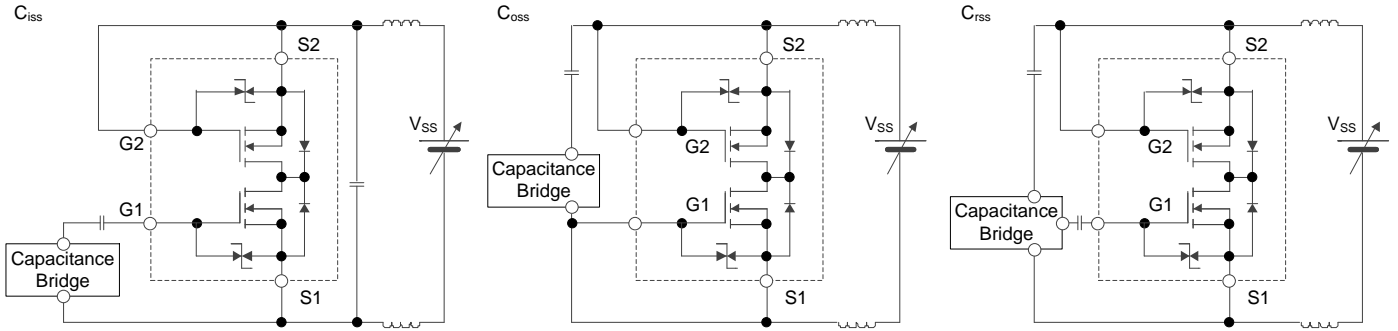


Test Circuit 5  $R_{SS(ON)}$   
 $V_{SS}/I_S$

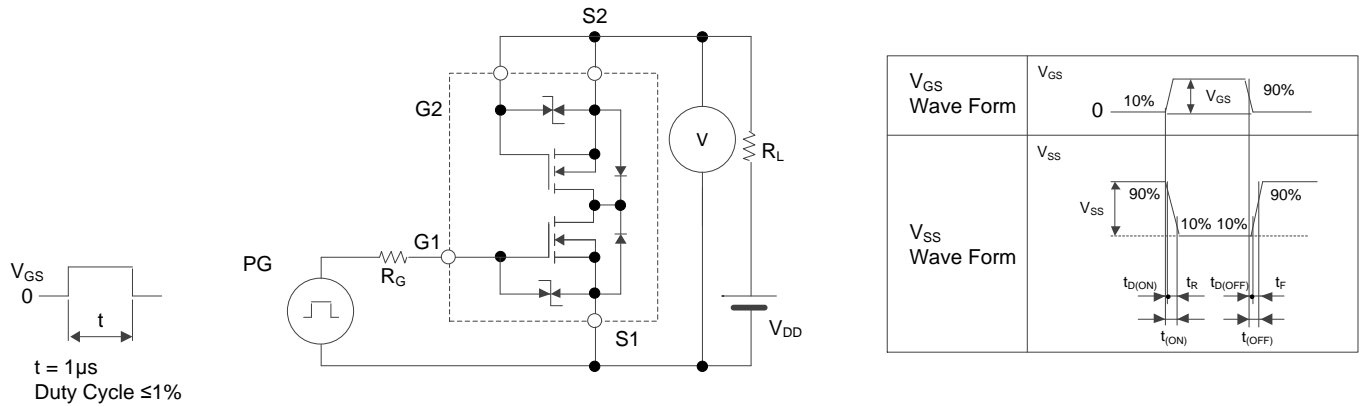


Test Circuit 6  $V_{F(S-S)}$   
When FET1 is measured, FET2 is added  $V_{GS} + 4.5V$ .

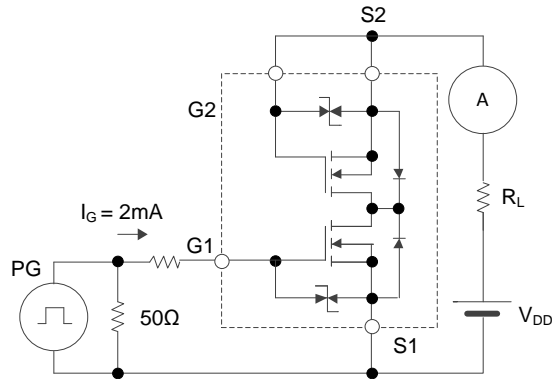
**Test Circuits (Cont.)**



Test Circuit 7



Test Circuit 8  $t_{D(ON)}$ ,  $t_R$ ,  $t_{D(OFF)}$ ,  $t_F$

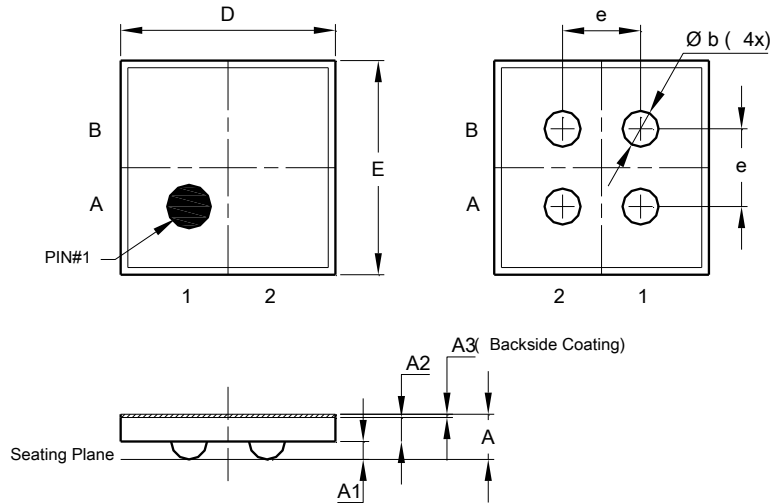


Test Circuit 9  $Q_G$

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X1-WLB1818-4

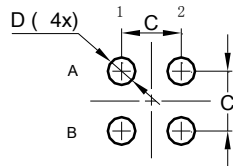


X1-WLB1818-4			
Dim	Min	Max	Typ
A	0.3420	0.4080	0.3750
A1	0.1350	0.1650	0.1500
A2	0.1850	0.2150	0.2000
A3	0.0220	0.0280	0.0250
b	0.2700	0.3300	0.3000
D	1.7800	1.8000	1.7900
E	1.7800	1.8000	1.7900
e	0.650 BSC		
<b>All Dimensions in mm</b>			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X1-WLB1818-4



Dimensions	Value (in mm)
C	0.65
D	0.30



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